# Tyler Creelan de Laguna

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## Education

**Bachelor of Science** in Computer Science with Honors, Oregon State University 2002

**Master of Science** in Computer Science, Oregon State University 2004

## Professional Activities

Google Developer Groups Portland 2022 - Current

**Chapter Head**

Chair of engineering association sponsored by Google for Developers. Lead six volunteer staff to organize symposiums for 1000+ members. Hosting seminars on algorithmics, probability, machine learning.

Microsoft TEALS 2023 - Current

**Computer Science Co-Teacher**

Teach advanced placement computer science A course (Java-based) at Lincoln High (Portland Public Schools), via non-profit volunteer program sponsored by Microsoft.

Career Break 2017 - 2022

Pause to travel internationally

Intel Corporation

**Software Design Engineer - Mobile** 2013 - 2017

Optimized design of the Intel Atom SoC, focus on low power interactions:

- Added experimental Linux kernel driver support for low-power Display Engine and frame compression in drm/i915 module, extending battery life to attain a prospective Internet of Things customer.
- Expanded LLVM-based framework (Maestro) to stress interconnect hardware (PCIE) with machine code.
- Rootcaused premature voltage phase shedding via Lauterbach and oscilloscope. Created microcode firmware patch to correct SVID bus signaling, resuming fab testing after $10k+ delay.

**Software Engineer - Modeling** 2010–2013

Developed control theory for i7 power controller (PCU) as extended tour of duty, owning memory (DDR):

- Modeled memory power limits (RAPL) and Turbo Burst algorithms in C++, comparing against microcode states with Coco. Created model in Specimen ‘e’ to find 11 firmware path bugs before tapein.
- Led taskforce for overlimit power spike; analyzed verilog to create experimental firmware patch and satisfy EU regulations for blade server customers, receiving Division Recognition award.

**Software Engineer - Post-Silicon Tools** 2004-2010

Team lead for power analysis of new CPUs, creating strategy at tape-in to meet biannual product qual:

- Built new Win7 app in Qt C++ for wattage telemetry, heading off 400mW routing bug in Xeon boards.
- Created new C++ test harness on host/target coupled with JTAG probe to verify S3 using cacheline breakpoints, discovered new circuit bug fixed in first Pentium XD product.
- Discovered catastrophic protocol bug in QuickPath Interconnect (QPI): prototyped solution with Focused Ion Beam edits: inserted fix in time for Core i7 launch, receiving achievement award.

## Open Source Contributions

- Advanced Component Platform Architecture (acpica.org): updated C-states (C, Linux, System states)
- Gnumeric (gnumeric.org), created Testmeric module (C++, gtk, glibc, sockets, TCP/IP).
- Debian GNU/Linux, Sarge Release (debian.org): archives, Bash, dpkg, automation

## Publications

1) "Power vs Debug: Solving IEEE JTAG Observability with Deep Powerdown™ (C6) active", Intel Design Technology and Test Conference (2007). T Creelan, N Ashraf and J Maxwell.

2) "Reporting CPU Frequency: The Challenge of Intel Turbo Boost™ Technology", Intel Design Technology and Test Conference (2007). T Creelan and T Baird.

3) "Scaling a Dataflow Testing Methodology", IEEE International Symposium on Software Reliability Engineering. (2006) p13-22. M Fisher, G Rothermel, T Creelan and M Burnett.

4) "Educators Have Hard Choices; Nationally". Science (Letters). Vol 289 (2000). Tyler Creelan.

## Certifications

Google: Project Management | Linux Debug: Intel Open Source Technology Center | Google: Python
Win10 Kernel Debug | PCIE-3, USB-3 - MindShare | Java Oracle Associate, in progress

## Professional Associations

Google Developer Groups Head | ACM ICPC Team | Microsoft TEALS | Google Student Groups Advisor
ACM Student Chapter Coach | Portland Java User Group | PDX Women In Technology Mentor

## Technical Skills

- **Software Programming Skills**: C/C++, Java, Bash, Python, Sus, Qt, Linux modules, x86 asm
- **Hardware Design and Debug Skills**: Specman, Intel microarchitecture, Test Access Port (TAP)
- **Operating Systems**: Debian GNU/Linux, Android
- **Interface Protocols**: Posix, Test Access Port (TAP), Joint Test Access Group (JTAG)
- **Tools**: Vim, IntelliJ, JMH, gcc, screen, WinDbg